AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A semiconductor integrated circuit apparatus comprising:

a nonvolatile storage provided with a memory array unit having a plurality of nonvolatile memory cells and a control unit for controlling write operation of storing information in the nonvolatile memory cells, read operation of reading out the information stored in the nonvolatile memory cells, and erase operation of erasing the information stored in the nonvolatile memory cells;

a volatile storage to be used as a work area of a program stored in the nonvolatile storage;

a central processing unit capable of executing a predetermined processing and giving instructions to the nonvolatile storage; and

a protect operation control unit for controlling the nonvolatile storage and the read operation of the nonvolatile storage, wherein

the memory array unit has a first protect memory area in which reading and writing of information stored are

prohibited under the control of the protect operation control unit;

the volatile storage has a second protect memory area in which reading from an area other than the first protect memory area of the memory array unit is prohibited under the control of the protect operation control unit; and

the second protect memory area of the volatile storage is used as a work area of a program stored in the first protect memory area of the nonvolatile storage.

2. (original) A semiconductor integrated circuit apparatus comprising:

a nonvolatile storage provided with a memory array unit having a plurality of nonvolatile memory cells and a control unit for controlling write operation of storing information in the nonvolatile memory cells, read operation of reading out the information stored in the nonvolatile memory cells, and erase operation of erasing the information stored in the nonvolatile memory cells;

a volatile storage;

a central processing unit capable of executing a predetermined processing and giving instructions to the nonvolatile storage; and

a protect operation control unit for controlling the nonvolatile storage and the read operation of the nonvolatile storage, wherein

the memory array unit has a first protect memory area in which reading and writing of information stored are prohibited under the control of the protect operation control unit; and

the volatile storage has a second protect memory area in which reading and writing from an area other than the first protect memory area of the memory array unit are prohibited under the control of the protect operation control unit.

3. (currently amended) The semiconductor integrated circuit apparatus according to claim 1~~ or 2~~, wherein

the protect operation control unit compares an address signal output from the central processing unit with a value of a program counter to judge whether or not the address signal is inside the first protect memory area.

4. (original) The semiconductor integrated circuit apparatus according to claim 3, wherein

the protect operation control unit compares an address signal output from the central processing unit with a value

of a program counter to permit reading in the first protect memory area only in the case where the address signal and the program counter value are address values inside the first protect memory area.

5. (currently amended) The semiconductor integrated circuit apparatus according to ~~any one of claims 1 to 4~~ claim 1, wherein

the protect operation control unit compares an address signal output from the central processing unit with a value of a program counter to judge whether or not the address signal is inside the second protect memory area.

6. (original) The semiconductor integrated circuit apparatus according to claim 5, wherein

the protect operation control unit compares an address signal output from the central processing unit with a value of a program counter to permit reading in the second protect memory area only in the case where the program counter value is inside the first protect memory area and the address signal is an address value inside the second protect memory area.

7. (currently amended) The semiconductor integrated circuit apparatus according to ~~any one of claims 1 to 6~~ claim 1, further comprising an erasure prohibition control unit for prohibiting erasure in the first protect memory area.

8. (original) The semiconductor integrated circuit apparatus according to claim 7, wherein

the erasure prohibition control unit is provided with

a key code generation circuit for outputting a previously set key code signal and

an erasure control circuit for prohibiting erasure in the first protect memory area when a key code signal generated by the key code generation circuit compares and coincides with a key code stored in the first protect memory area in the case where erasure operation of the memory array unit occurs.

9. (currently amended) The semiconductor integrated circuit apparatus according to ~~any one of claims 1 to 8~~ claim 1, further comprising an rewrite prohibition control unit for prohibiting rewrite in the first protect memory area.

10. (original) The semiconductor integrated circuit apparatus according to claim 9, wherein

the rewrite prohibition control unit is provided with:

a key code generation circuit for outputting a previously set key code signal;

an address judgment unit for judging whether or not the rewrite destination address signal is in the first protect memory area;

a key code judgment unit for comparing a key code signal generated by the key code generation circuit and a key code stored in the first protect memory area and outputting a coincidence signal when the key codes coincide with each other; and

a rewrite control circuit for outputting a rewrite prohibition signal for prohibiting rewrite in the first protect memory area in the case where the rewrite destination address signal is in the first protect memory area and the key codes coincide with each other when rewrite operation of the memory array unit occurs.

11. (original) An electric system comprising:

a nonvolatile semiconductor storage apparatus provided with a nonvolatile storage provided with a memory array unit having a plurality of nonvolatile memory cells and a control

unit for controlling write operation of storing information in the nonvolatile memory cells, read operation of reading out the information stored in the nonvolatile memory cells, and erase operation of erasing the information stored in the nonvolatile memory cells;

a volatile semiconductor storage apparatus to be used as a work area of a program stored in the nonvolatile semiconductor storage apparatus;

a semiconductor integrated circuit apparatus provided with a central processing unit capable of executing a predetermined processing and giving instructions to the nonvolatile semiconductor storage apparatus and a protect operation control unit for controlling the nonvolatile semiconductor storage apparatus and the read operation of the volatile semiconductor storage apparatus, wherein

the memory array unit has a first protect memory area in which reading of information stored is prohibited under the control of the protect operation control unit;

the volatile semiconductor storage apparatus has a second protect memory area in which reading from an area other than the first protect memory area of the memory array unit is prohibited under the control of the protect operation control unit; and

the second protect memory area is used as a work area of a program stored in the nonvolatile semiconductor storage apparatus.

12. (original) The electric system according to claim 11, wherein

the protect operation control unit compares an address signal output from the central processing unit with a value of a program counter to judge whether or not the address signal is inside the first and the second protect memory areas.

13. (original) The electric system according to claim 12, wherein

the protect operation control unit compares an address signal output from the central processing unit with a value of a program counter to permit reading in the first protect memory area in the case where the address signal and the program counter value are address values inside the first protect memory area and to permit reading in the second protect memory area in the case where the address signal is an address value inside the second protect memory area.

14. (currently amended) The electric system according to ~~any one of claims 10 to 13~~ claim 11, further comprising an erasure prohibition control unit for prohibiting erasure in the first protect memory area.

15. (currently amended) The electric system according to ~~any one of claims 10 to 14~~ claim 11, further comprising a rewrite prohibition control unit for prohibiting rewrite in the first protect memory area.

16. (new) The semiconductor integrated circuit apparatus according to claim 2, wherein

the protect operation control unit compares an address signal output from the central processing unit with a value of a program counter to judge whether or not the address signal is inside the first protect memory area.

17. (new) The semiconductor integrated circuit apparatus according to claim 16, wherein

the protect operation control unit compares an address signal output from the central processing unit with a value of a program counter to permit reading in the first protect memory area only in the case where the address signal and

the program counter value are address values inside the first protect memory area.

18. (new) The semiconductor integrated circuit apparatus according to claim 2, wherein

the protect operation control unit compares an address signal output from the central processing unit with a value of a program counter to judge whether or not the address signal is inside the second protect memory area.

19. (new) The semiconductor integrated circuit apparatus according to claim 18, wherein

the protect operation control unit compares an address signal output from the central processing unit with a value of a program counter to permit reading in the second protect memory area only in the case where the program counter value is inside the first protect memory area and the address signal is an address value inside the second protect memory area.

20. (new) The semiconductor integrated circuit apparatus according to claim 2, further comprising an erasure prohibition control unit for prohibiting erasure in the first protect memory area.

21. (new) The semiconductor integrated circuit apparatus according to claim 20, wherein

the erasure prohibition control unit is provided with

a key code generation circuit for outputting a previously set key code signal and

an erasure control circuit for prohibiting erasure in the first protect memory area when a key code signal generated by the key code generation circuit compares and coincides with a key code stored in the first protect memory area in the case where erasure operation of the memory array unit occurs.

22. (new) The semiconductor integrated circuit apparatus according to claim 2, further comprising an rewrite prohibition control unit for prohibiting rewrite in the first protect memory area.

23. (new) The semiconductor integrated circuit apparatus according to claim 22, wherein

the rewrite prohibition control unit is provided with:

a key code generation circuit for outputting a previously set key code signal;

an address judgment unit for judging whether or not the rewrite destination address signal is in the first protect memory area;

a key code judgment unit for comparing a key code signal generated by the key code generation circuit and a key code stored in the first protect memory area and outputting a coincidence signal when the key codes coincide with each other; and

a rewrite control circuit for outputting a rewrite prohibition signal for prohibiting rewrite in the first protect memory area in the case where the rewrite destination address signal is in the first protect memory area and the key codes coincide with each other when rewrite operation of the memory array unit occurs.